UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,250	10/14/2003	Benjamin Thomas Percer	200207855-1	3994

22879 7590 03/16/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
BROWN, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,250	PERCER ET AL.	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/03, 2/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on 10/14/2003 and 2/24/2005 were filed. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

2. The information disclosure statement filed 9/19/2005 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the application number does not match the application number of the present application. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4-14, 22, 25-32, and 35-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Parrett(US Patent 5,586,271).

As to claim 1, Parrett discloses a bus interface control for selectively supplying pull-up voltage to signal lines of a bus(bus 11c, see Fig. 1a), comprising a plurality of pull-up circuits(isolation disconnect circuits12a-12g, see Fig. 1a), each connected to one of the signal lines and isolated from the other pull-up circuits to prevent signals from the one of the signal lines passing through the pull-up circuit to another one of the signal lines, and a multi-mode power source(power supply 15, see Fig. 2a) that, in a first power mode, powers the plurality of pull-up circuits and, in a second power mode, does not power the plurality of pull-up circuits.

As to claim 4, Parrett discloses the bus interface control wherein the power mode is responsive to an enable signal of the bus(see column 5, line 61- column 6, line 3).

As to claim 5, Parrett discloses the bus interface control wherein the multi-mode power source comprises a voltage regulator that can be selectively enabled by a voltage regulator enable signal(see column 5, line 61- column 6, line 3).

As to claim 6, Parrett discloses the bus interface control wherein the multi-mode power source comprises a switch circuit(select switch 18, see Fig. 2c) between a power source and the plurality of pull-up circuits.

As to claim 7, Parrett discloses the bus interface control wherein the switch circuit comprises a field-effect transistor(see column 7, lines 36-38).

As to claim 8, Parrett discloses the bus interface control further comprising a

switchable bus bridge(adapter 17, see Fig. 2c) that is capable of operating in at least two bridging modes and, in a first bridging mode, connects at least some of the signal lines to a second bus and, in a second bridging mode, does not connect at least some of the signal lines to the second bus.

As to claim 9, Parrett discloses the bus interface control wherein the bridging mode is responsive to an enable signal of the bus(see column 5, line 61- column 6, line 3).

As to claim 10, Parrett discloses the bus interface control wherein the power mode is responsive to the enable signal of the bus(see column 5, line 61- column 6, line 3).

As to claim 11, Parrett discloses the bus interface control wherein the plurality of pull-up circuits, the multi-mode power source and the switchable bus bridge are co-located on a removable circuit board(see column 6, lines 62-66).

As to claim 12, Parrett discloses the bus interface control wherein the bus is a Compact PCI bus(see column 4, lines 51-54).

As to claim 13, Parrett discloses the bus interface control wherein the plurality of pull-up circuits and the multi-mode power source are implemented in a single integrated circuit(see column 6, lines 53-58).

As to claim 14, Parrett discloses the bus interface control wherein the single integrated circuit further comprises a switchable bus bridge(adapter 17, see Fig. 2c) that is capable of operating in at least two bridging modes and, in a first bridging mode, connects at least some of the signal lines to a second bus and, in a second bridging

mode, does not connect at least some of the signal lines to the second bus.

As to claim 22, Parrett discloses a bus interface control for controlling an interface to a bus having a plurality of signal lines, comprising isolation means(isolation disconnect circuits12c-12g, see Fig. 1b) for isolating each of the signal lines of the bus from other signal lines of the bus, and pull-up means(power supply 15, see Fig. 2c) for selectively providing pull-up voltage to each of the signal lines of the bus.

As to claim 25, Parrett discloses the bus interface wherein the pull-up means comprises a voltage regulator that can be selectively enabled by a voltage regulator enable signal(see column 5, line 61- column 6, line 3).

As to claim 26, Parrett discloses the bus interface control wherein the isolation means is controlled based on an enable signal of the bus(see column 5, line 61- column 6, line 3).

As to claim 27, Parrett discloses the bus interface control wherein the pull-up means comprises a switch circuit(select switch 18, see Fig. 2c) between a power source and the signal lines.

As to claim 28, Parrett discloses the bus interface control wherein the switch circuit comprises a field-effect transition(see column 7, lines 36-38).

As to claim 29, Parrett discloses the bus interface control further comprising bus bridge means(adapter 17, see Fig. 2c) for selectively bridging at least some of the plurality of signal lines of the bus to a second bus.

As to claim 30, Parrett discloses the bus interface control wherein the bus bridge means is controlled based on an enable signal of the bus(see column 5, line 61- column

6, line 3).

As to claim 31, Parrett discloses the bus interface control wherein the bus is a Compact PCI bus(see column 4, lines 51-54).

As to claim 32, Parrett discloses a method of controlling an interface to a bus having a plurality of signal lines, comprising in one power mode, providing pull-up voltage to each of the signal lines(see column 7, lines 36-43) and, in another power mode, not providing the pull-up voltage(see column 8, lines 2-5), and isolating each of the plurality of signal lines from other signal lines to prevent signals from any of the signal lines passing to another signal line(see column 3, lines 40-43).

As to claim 35, Parrett discloses the method further comprising determining the power mode based on an enable signal of the bus(see column 5, line 61- column 6, line 3).

As to claim 36, Parrett discloses the method wherein the providing pull-up voltage comprises enabling a multi-mode power source connected to the plurality of signal lines of the bus(see column 5, line 61- column 6, line 3).

As to claim 37, Parrett discloses the method wherein the multi-mode power source comprises a voltage regulator that can be selectively enabled by a voltage regulator enable signal(see column 5, line 61- column 6, line 3).

As to claim 38, Parrett discloses the method wherein the multi-mode power source comprises a switch circuit(select switch 18, see Fig. 2c) between a power source and the plurality of signal lines of the bus.

As to claim 39, Parrett discloses the method wherein the switch circuit comprises

a field-effect transistor(see column 7, lines 36-38).

As to claim 40, Parrett discloses the method further comprising in a first bridging mode, bridging at least some of the plurality of signal lines to a second bus and, in another bridging mode, not bridging the at least some of the signal lines to the second bus(see column 6, lines 62-66).

As to claim 41, Parrett discloses the method further comprising determining the bridging mode based on an enable signal of the bus(see column 5, line 61- column 6, line 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 2, 3, 15-21, 23, 24, 33, 34, and 42-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrett(US Patent 5,586,271) further in view of Graves(US Patent 6,414,533).

As to claim 2, Parrett discloses the bus interface control as cited in claim 1 and explained above. However Parrett fails to disclose the bus interface control where each pull-up circuit is isolated from the other pull-up circuits by a diode.

Graves teaches the bus interface control wherein each pull-up circuit is isolated from the other pull-up circuits by a diode(Schottky diode D1, see Fig. 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Parrett and Graves in order to implement a pull-up circuit consisting of a diode to isolate pull-up circuits from one another. The motivation to do so would be to have a bus interface control that can isolate a board from a bus without requiring extensive real estate on the board.

As to claim 3, Parrett discloses the bus interface control as cited in claim 1 and explained above. However, Parrett fails to disclose the bus interface control wherein each pull-up circuit is isolated from the other pull-up circuits by a Schottky diode.

Graves teaches the bus interface control wherein each pull-up circuit is isolated from the other pull-up circuits by a Schottky diode(Schottky diode D1, see Fig. 3).

As to claim 15, Parrett discloses a bus interface control for selectively connecting signal lines of a first bus(buses 11i, see Fig. 1b) to a second bus(bus 11c, see Fig. 1b), comprising a plurality of pull-up circuits(isolation disconnect circuits12c-12g, see Fig. 1b), each connected to one of the signal lines of the first bus and isolated from the other

pull-up circuits to prevent signals from the one of the signal lines of the first bus passing through the pull-up circuit to another one of the signal lines of the first bus. Parrett also discloses a voltage regulator(power supply 15, see Fig. 2c) that can be selectively enabled by a voltage regulator enable signal and that, in a first power mode, powers the plurality of pull-up circuits and, in a second power mode, does not power the plurality of pull-up circuits, wherein the power mode is responsive to an enable signal of the first bus, and a switchable bus bridge(adapter 17, see Fig. 2c) that is capable of operating in at least two bridging modes and, in a first bridging mode, connects at least some of the signal lines of the first bus to the second bus and, in a second bridging mode, does not connect at least some of the signal lines of the first bus to the second bus, wherein the bridging mode is responsive to the enable signal of the first bus. However, Parrett fails to discloses the pull-up circuits being isolated by a diode.

Graves teaches the pull-up circuits being isolated by a diode(Schottky diode D1, see Fig. 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Parrett and Graves in order to implement a pull-up circuit consisting of a diode to isolate pull-up circuits from one another. The motivation to do so would be to have a bus interface control that can isolate a board from a bus without requiring extensive real estate on the board.

As to claim 16, Parrett discloses the bus interface control wherein the bus is a Compact PCI bus(see column 4, lines 51-54).

As to claim 17, Graves teaches the bus interface control wherein the diode is a Schottky diode(Schottky diode D1, see Fig. 3).

As to claim 18, Parrett discloses a bus interface control for selectively connecting signal lines of a first bus(buses 11i, see Fig. 1b) to a second bus(bus 11c, see Fig. 1b), comprising a plurality of pull-up circuits(isolation disconnect circuits12c-12g, see Fig. 1b), each connected to one of the signal lines of the first bus and isolated from the other pull-up circuits to prevent signals from the one of the signal lines of the first bus passing through the pull-up circuit to another one of the signal lines of the first bus. Parrett also discloses a switch circuit(select switch 18, see Fig. 2c) between a power source and the plurality of pull-up circuits that, in a first power mode, powers the plurality of pull-up circuits and, in a second power mode, does not power the plurality of pull-up circuits, wherein the power mode is responsive to an enable signal of the first bus, and a switchable bus bridge(adapter 17, see Fig. 2c) that is capable of operating in at least two bridging modes and, in a first bridging mode, connects at least some of the signal lines of the first bus to the second bus and, in a second bridging mode, does not connect at least some of the signal lines of the first bus to the second bus, wherein the bridging mode is responsive to the enable signal of the first bus. However, Parrett fails to discloses the pull-up circuits being isolated by a diode.

Graves teaches the pull-up circuits being isolated by a diode(Schottky diode D1, see Fig. 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Parrett and Graves in order to implement a pull-up circuit consisting of a diode to isolate pull-up circuits from one another. The motivation to do so would be to have a bus interface control that can isolate a board from a bus without requiring extensive real estate on the board.

As to claim 19, Parrett discloses the bus interface control wherein the bus is a Compact PCI bus(see column 4, lines 51-54).

As to claim 20, Graves teaches the bus interface control wherein the diode is a Schottky diode(Schottky diode D1, see Fig. 3).

As to claim 21, Parrett discloses the bus interface control wherein the switch circuit comprises a field-effect transistor(see column 7, lines 36-38).

As to claim 23, Parrett discloses the bus interface control as cited in claim 22 and explained above. However, Parrett fails to disclose the bus interface control wherein the isolation means comprise a diode.

Graves teaches the bus interface control wherein the isolation means comprises a diode(Schottky diode D1, see Fig. 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Parrett and Graves in order to implement a pull-up circuit consisting of a diode to isolate pull-up circuits from one another. The motivation to do so would be to have a bus interface control that can isolate a board from a bus without requiring extensive real estate on the board.

As to claim 24, Parrett discloses the bus interface control as cited in claim 22 and explained above. However, Parrett fails to disclose the bus interface control wherein the isolation means comprise a Schottky diode.

Graves teaches the bus interface control wherein the isolation means comprises a Schottky diode(Schottky diode D1, see Fig. 3).

As to claim 33, Parrett discloses the method as cited in claim 32 and explained

above. However, Parrett fails to disclose the method wherein isolating comprises blocking a signal with a diode.

Graves teaches the method wherein isolating comprises blocking a signal with a diode(Schottky diode D1, see Fig. 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Parrett and Graves in order to implement a method to isolate pull-up circuits from one another using a diode. The motivation to do so would be to have a method that can isolate a board from a bus without requiring extensive real estate on the board.

As to claim 34, Parrett discloses the method as cited in claim 32 and explained above. However, Parrett fails to disclose the method wherein isolating comprises blocking a signal with a Schottky diode.

Graves teaches the method wherein isolating comprises blocking a signal with a Schottky diode(Schottky diode D1, see Fig. 3).

As to claim 42, Parrett discloses a bus interface control for selectively supplying pull-up voltage to signal lines of a bus, comprising a multi-mode power source(power source 15, see Fig. 2c) capable of operating in at least two power modes, and a plurality of pull-up circuits(isolation disconnect circuits12c-12g, see Fig. 1b), each connected between one of the signal lines and the multi-mode power source wherein, in a first power mode, the multi-mode power source powers the plurality of pull-up circuits and, in a second power mode, the multi-mode power source does not power the plurality of pull-up circuits. However, Parrett fails to disclose a plurality of diodes, each connected in series with one of the plurality of pull-up circuits and between one of the signal lines

and the multi-mode power source and, thereby preventing current flowing in one direction through the one of the plurality of pull-up circuits.

Graves teaches a plurality of diodes(Schottky diode D1, see Fig. 3), each connected in series with one of the plurality of pull-up circuits and between one of the signal lines and the multi-mode power source and, thereby preventing current flowing in one direction through the one of the plurality of pull-up circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Parrett and Graves in order to implement a pull-up circuit consisting of a diode to isolate pull-up circuits from one another. The motivation to do so would be to have a bus interface control that can isolate a board from a bus without requiring extensive real estate on the board.

As to claim 43, Graves teaches the bus interface control wherein each diode comprises a Schottky diode(Schottky diode D1, see Fig. 3).

As to claim 44, Parrett discloses the bus interface control wherein the multi-mode power source comprises a voltage regulator having a voltage regulator enable signal input connected to an enable signal of the bus(see column 5, line 61- column 6, line 3).

As to claim 45, Parrett discloses the bus interface control wherein the multi-mode power source comprises a power source(power source 15, see Fig. 2c), and a switch circuit(select switch 18, see Fig. 2c) between the power source and the plurality of pull-up circuits, wherein the switch circuit has a switch circuit enable signal input connected to an enable signal of the bus.

As to claim 46, Parrett discloses the bus interface control further comprising a

switchable bus bridge(adapter 17, see Fig. 2c) connected between the signal lines and a second bus, wherein the switchable bus bridge is capable of operating in at least two bridging modes and has a bridge enable signal input connected to an enable signal of the bus, whereby in a first bridging mode, the switchable bus bridge connects at least some of the signal lines to the second bus and, in a second bridging mode, the switchable bus bridge does not connect at least some of the signal lines to the second bus.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Brown whose telephone number is (571)272-5932. The examiner can normally be reached on Monday-Friday from 7:00am to 3:30pm(EST).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIRS) system. Status information for the published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications are available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 886-217-9197 (toll-free).

Michael J. Brown
Art Unit 2116

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100